**Name of the Faculty** **:** Ms. Monika Gaur

**Discipline** **:** CSE

**Semester** **: 6th**

**Subject**  **:** Digital System Design

**Lesson Plan Duration** **:** 15 weeks (from January, 2019 to April, 2019)

**\*\* Work Load (Lecture / Practical) per week (in hours): Lectures-03, Practicals-02**

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| **Week** | **Theory** | | **Practical** | |
|  | **Lecture day** | **Topic**  **(including assignment / test)** | **Practical day** | **Topic** |
| 1st | 1st | * Introduction to CAD tools for digital system hardware description languages | 1st | Design all gates using VHDL. |
| 2nd | * Introduction to VHDL |  |  |
| 3rd | * VHDL data objects, Classes |  |  |
| 2nd | 4th | * Data types | 2nd | Write VHDL programs for the following circuits, check the wave forms and the hardware generated  half adder, Full adder |
| 5th | * Operators, Logical operators |  |  |
| 6th | * Overloading, delay |  |  |
| 3rd | 7th | * Introduction to behavioral data flow and structural models | 3rd | Write VHDL programs for the following circuits, check the wave forms and the hardware generated  a. multiplexer  b. Demultiplexer |
| 8th | * Assignment statements, Sequential statement |  |  |
| 9th | * Process, Conditional statement |  |  |
| 4th | 10th | * Case statement ,array and loop | 4th | Write VHDL programs for the following circuits, check the wave forms and the hardware generated  a. decoder  b. encoder |
| 11th | * Resolution function, Packages |  |  |
| 12th | * Libraries |  |  |
| 5th | 13th | * Concurrent statements, subprograms: application of function and procedures | 5th | Write a VHDL program for a comparator and check the wave forms and the hardware generated |
| 14th | * Structural Modeling, component declaration, structural layout |  |  |
| 15th | * Generics VHDL Models & simulation of MUX |  |  |
| 6th | 16th | * Models &simulation of DEMUX, Models & simulation of encoder | 6th | Write a VHDL program for a code converter and check the wave forms and the hardware generated |
| 17th | * Models &simulation of Decoder, Models &simulation of code convertor |  |  |
| 18th | * Implementation of Boolean function, |  |  |
| 7th | 19th | * Models &simulation D flip flop, T flip flop | 7th | Write a VHDL program for a S-R FLIP-FLOP and check the wave forms and the hardware generated |
| 20th | * Models &simulation of JK,SR FF |  |  |
| 21st | * Models of 4-Bit register serial in and parallel out shift register |  |  |
| 8th | 22nd | * simulation of 4-Bit register serial in and parallel out shift register | 8th | Write a VHDL program for a counter and check the wave forms and the hardware generated |
| 23rd | * Models of 4-Bit register parallel in and parallel out shift register |  |  |
| 24th | * simulation of 4-Bit register parallel in and parallel out shift register |  |  |
| 9th | 25th | * Models of 4-Bit up counter,4 bit down counter | 9th | Write VHDL programs for the following circuits, check the wave forms and the hardware generated  a. register  b. shift register |
| 26th | * simulation of 4-Bit up counter,4 bit down counter |  |  |
| 27th | * Models of 4-Bit up counter |  |  |
| 10th | 28th | * Models of 4-Bit down counter | 10th | Write VHDL programs for the following circuits, check the wave forms and the hardware generated  a. half subtractor  b. full subtractor |
| 29th | * simulation of 4-Bit up counter |  |  |
| 30th | * simulation of 4-Bit down counter |  |  |
| 11th | 31st | * Models &simulation of 4-Bit register serial in and serial out right shift register | 11th | Write VHDL programs for the J-K Flip Flop ,check the wave forms |
| 32nd | * 4-Bit up-down counter |  |  |
| 33rd | * Basic components of a computer specification |  |  |
| 12th | 34th | * Architecture of a simple microcomputer system | 12th | Write VHDL programs for the D Flip Flop ,check the wave forms |
| 35th | * Implementation of simple microcomputer using ROM |  |  |
| 36th | * Implementation of simple microcomputer using PLA's |  |  |
| 13th | 37th | * PAL | 13th | Write VHDL programs for the T Flip Flop ,check the wave forms |
| 38th | * GAL |  |  |
| 39th | * PEEL |  |  |
| 14th | 40th | * CPLD | 14th | Write VHDL programs for the seven segment display, check the wave forms |
| 41st | * FPGA |  |  |
| 42nd | * Design implementation using CPLD |  |  |
| 15th | 43rd | * Design implementation using FPGA | 15th | Design a arithmetic unit. |
| 44th | * Revision |  |  |
| 45th | * Revision |  |  |